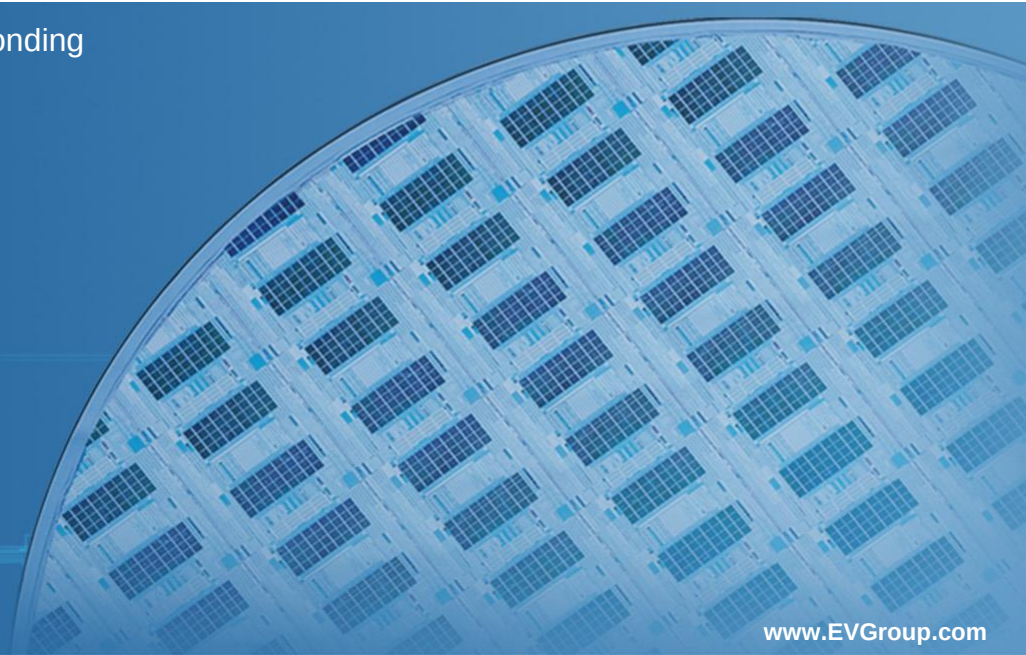
37th Chemnitz Seminar

Die-to-Wafer Bonding

Tobias Wernicke – Process Technology Manager – Bonding



Outline

- Introduction
- Process Overview
- Process Features and results
  - Direct placement
  - D2W
  - CD2W
- Summary & Outlook

Introduction

Why?

Super Chip

Manufacturing Needs | HD Chiplet Integration

Interconnect Scaling

Yield Optimization

Hybrid D2W / W2W Bonding

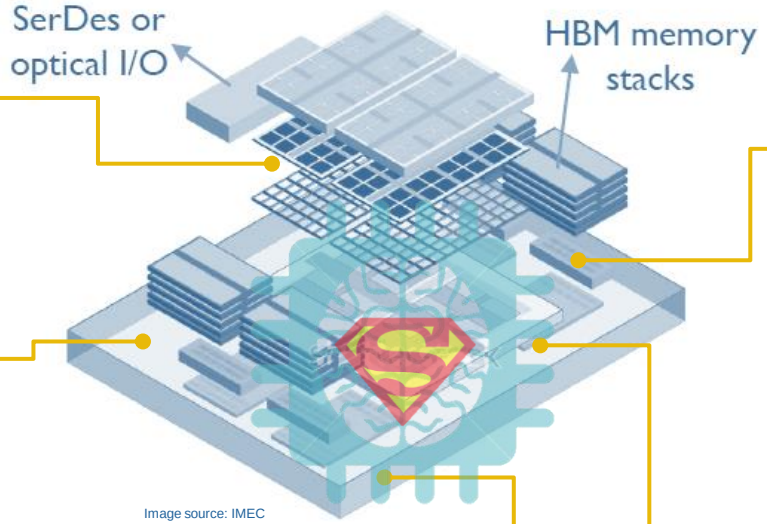


Image source: IMEC

Die-Level Metrology

Adaptive Patterning for High Density RDL

Smaller Form Factor

Support during Device Thinning

Assembly

Warpage Control

EVG Equipment Solutions | 3D Integration Portfolio

„Scaling Boosters“

EVG40NT2
W2W, D2W and D2D Overlay Metrology for organic and Inorganic Dies and wafers

EVG Nanocleave
Selective and full area IR Laser release through silicon

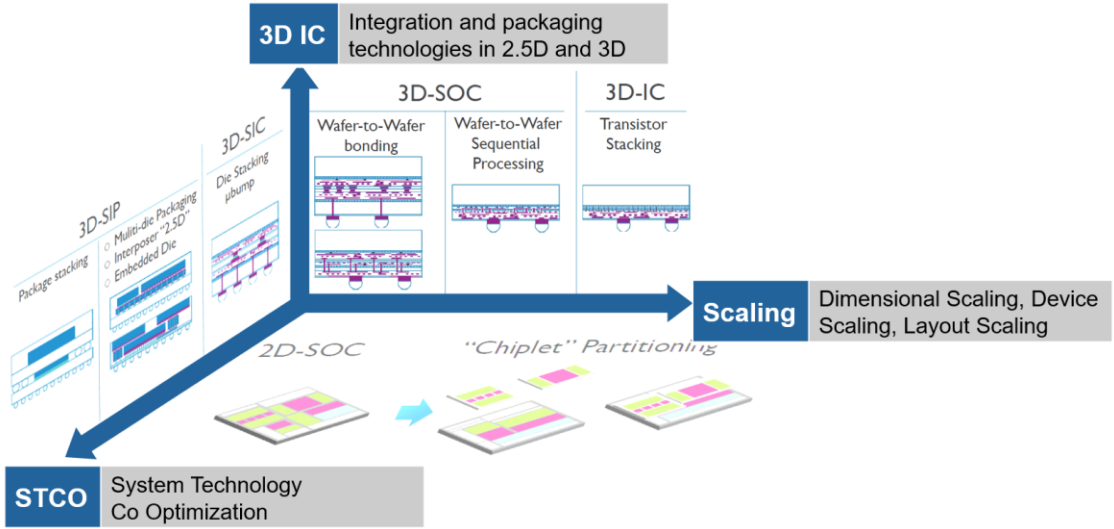
EVG GEMINI FB XT
Hybrid Bonding of two FEOL metallization circuits <100nm overlay

EVG BONDSCALE
Combination of wafer-to-wafer bonding and EUV or Immersion lithography

EVG320D2W
D2W Fusion and Hybrid Bonding using CoD2W or DPD2W flows

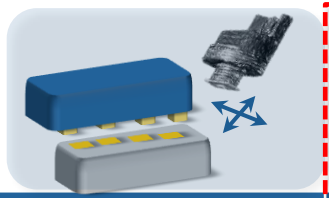
EVG Lithoscale
Fully digital maskless Lithography for Adaptive patterning Rapid prototyping & fully traceable chiplets

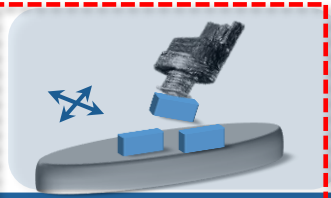
EVG850 TB/DB
Temporary Bonding & Debonding for next FoWLP, 2.5D and 3D processes

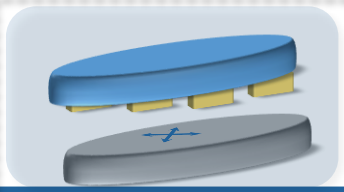


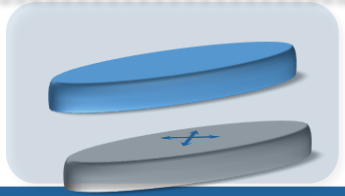
Process Overview

Die - to - Die vs. Wafer to Wafer









Stacking Method	Chip to Chip	Chip to Wafer	Collective Die to Wafer	Wafer to Wafer
Throughput	Low	Low	High	High
Yield	High*	High*	High*	Mid
Application	Packaging	Processor, Memory, Mems	Image Sensor, Processor, Memory, Mems	Image Sensor, Processor, Memory, Mems
Alignment	1 µm**	1 µm**	1 µm**	100 nm
Challenges	Alignment accuracy Cleanliness / Plasma Throughput	Alignment accuracy Cleanliness / Plasma Throughput	Yield	Yield Heterogeneous integration
Compatibility Hybrid Bonding	Mid	Mid	Yes ***	yes
		Improved yield and throughput management	Improved yield and throughput management	High yield application

* Known good dies
** Development for 200 nm
*** HVM for III-V Die transfer

Direct Placement (DP-D2W) Bonding | Process Flow

Transfer Method	Pro's	Con's	Maturity
DP-D2W Direct placement of activated dies using Flip Chip Bonder	• Versatile method • Die thickness variation	• Die handling especially for multi die stacks such as SRAM, DRAM • Particle management during die placement	• Feasibility testing required and ongoing

EVG320D2W | Baseline Configuration

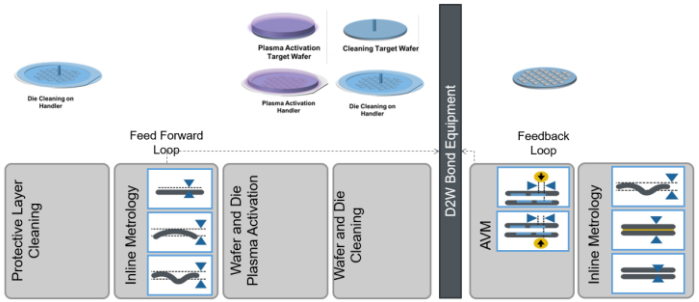
- Automated Single D2W preparation and activation system
  - Provides seamless integration with third-party die bonders
  - Enables plasma activation and cleaning of dies on 12” filmframe as preparation for further direct placement fusion bond process

- Modular concept for 12” filmframe and/or 300mm wafer
  - LowTemp Plasma Activation Module
  - Clean Module for Fusion Bonding
  - UV Expose Module

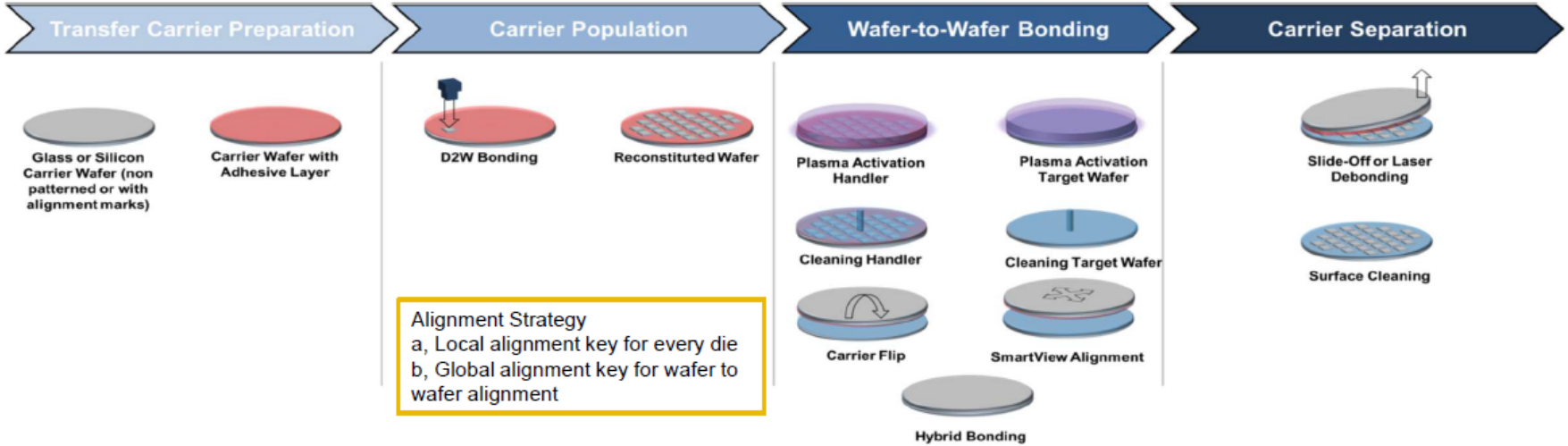
- Customer configuration based on process requirements and purpose (e.g. R&D)

- (Optional integration to die bonder)

EVG®320 D2W Die Activation and Cleaning



Collective Die-to-Wafer (Co-D2W) Bonding | Process Flow

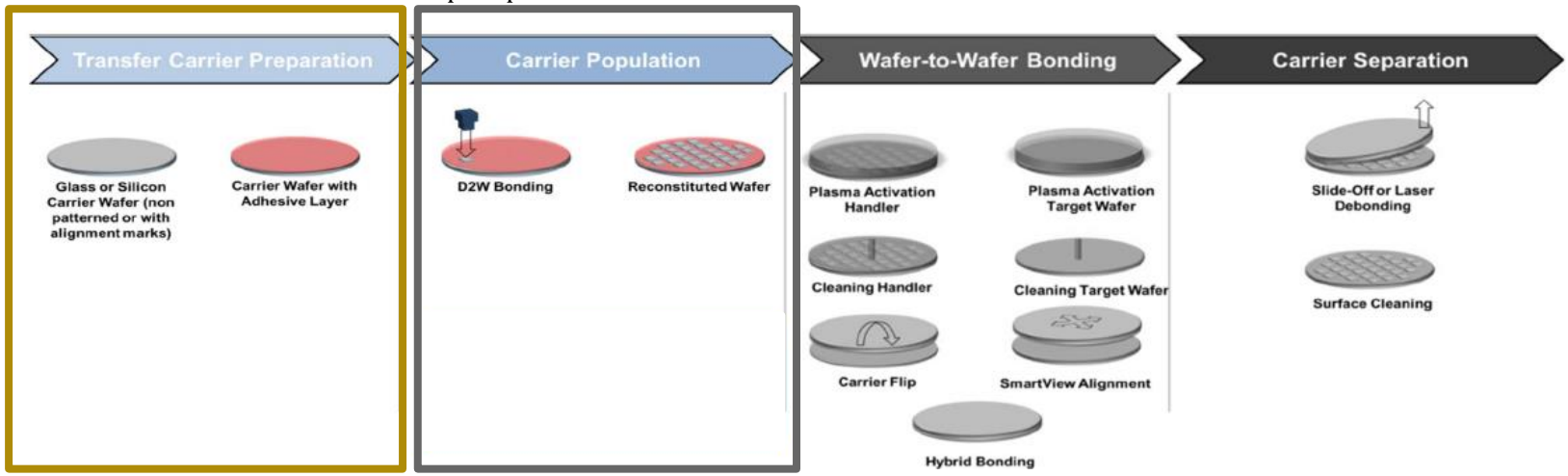


Transfer Method	Pro's	Con's	Maturity Level
Collective Die Transfer by Reconstituted Carrier	• Proven technology • Die activation and cleaning equivalent to W2W hybrid bonding • Oxide management • Reuse of carrier feasible	• Error propagation of D2W + W2W alignment • Cost of carrier prep, utilization and clean • Die thickness needs to be in narrow range	High Volume production proven for several years

Collective Die-to-Wafer (Co-D2W) Bonding | Process Flow

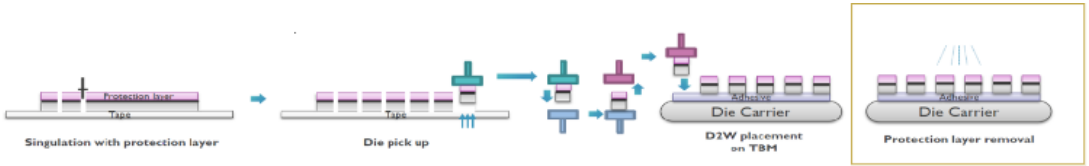
Collective Die Carrier Preparation

EVG®101 Flip Chip Bonder



EVG®101

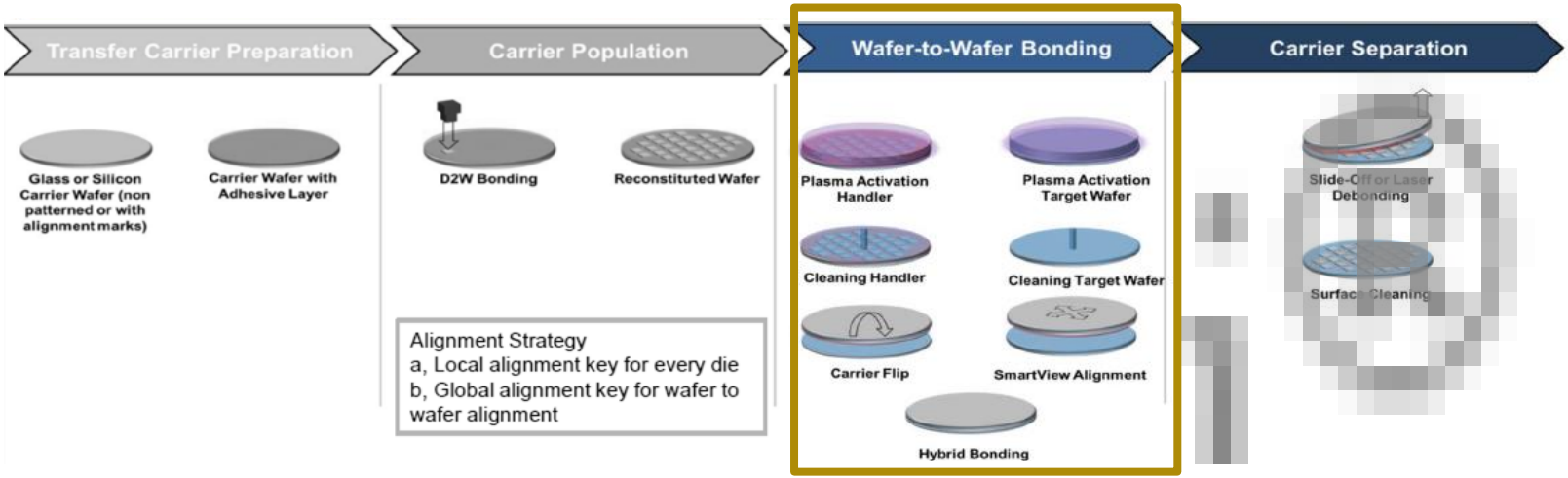
- A protective layer is applied on top of the dies to prevent the contamination of the die surface during the dicing and carrier population processes.



Collective Die-to-Wafer (Co-D2W) Bonding | Process Flow

Collective Die to Wafer Bonding

Gemini®

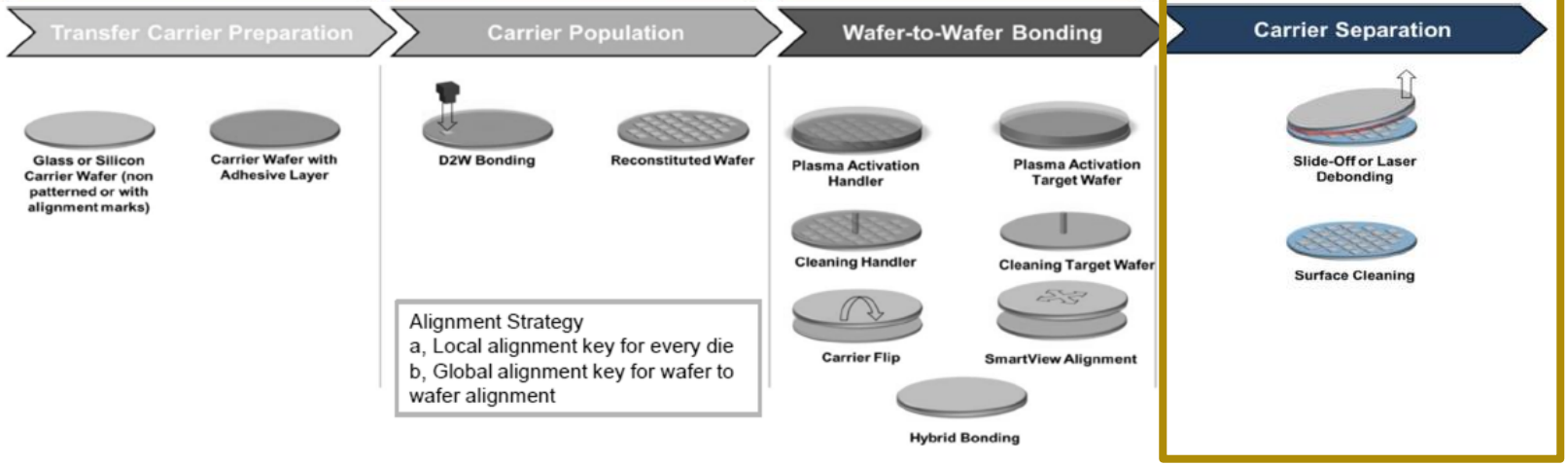


- The D2W bonding is preformed at wafer level using the same W2W bonding systems.

Gemini®

Collective Die-to-Wafer (Co-D2W) Bonding | Process Flow

Die transfer process



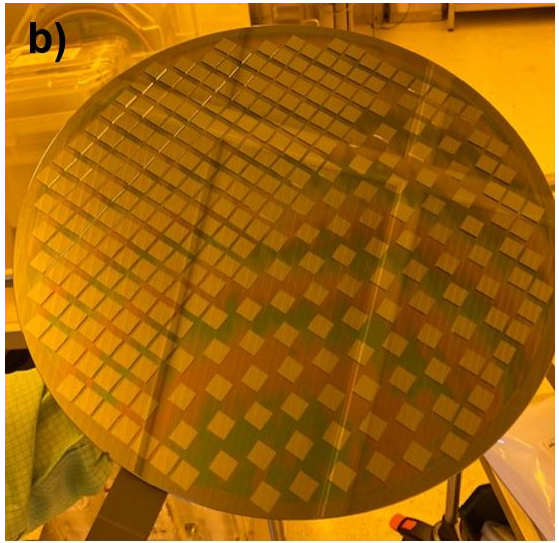
EVG850®

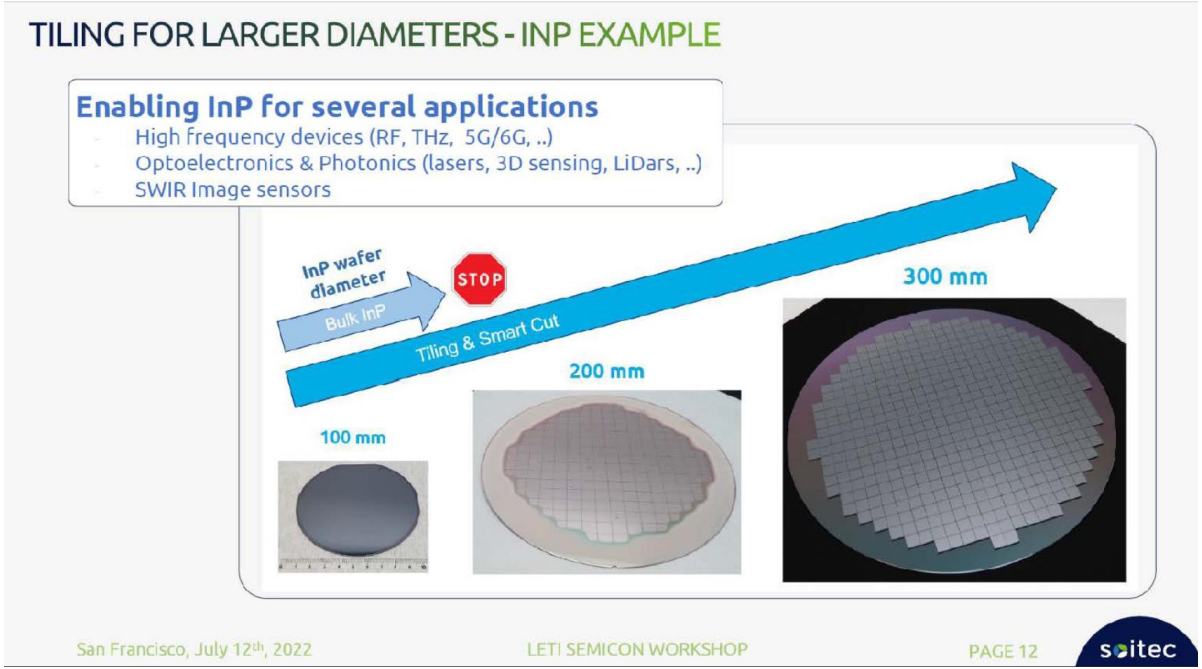
EVG850®

D2W Bonding – Process Results

DP-D2W Bonding | III-V Integration on 300mm Wafers

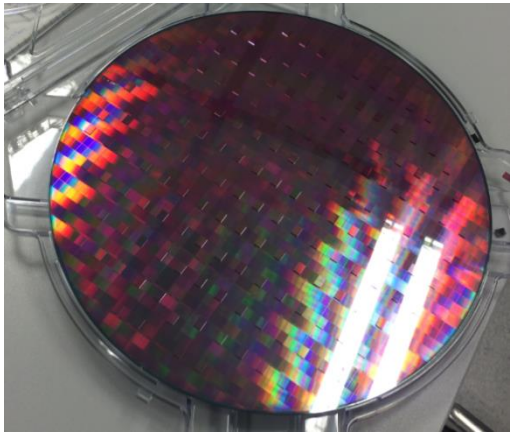
- Populating a 300mm Silicon wafers with 10 mm x 10mm InP dies succesfully demonstrated
- Usage of full backplane area possible
- No limitation of growth substrate sizes

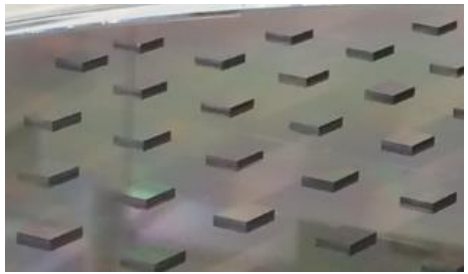




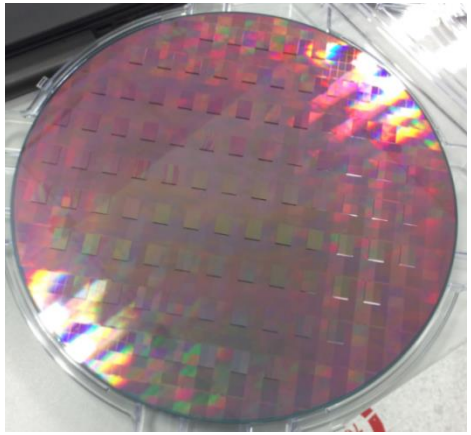
Co-D2W Bonding | Process Results – Hybrid Bonding

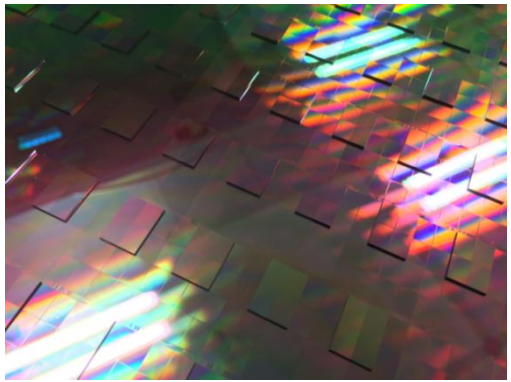
Demonstrator A - 300mm Hybrid Bonding
5mmx7mm





Demonstrator B - 300mm Hybrid Bonding
10mmx14mm

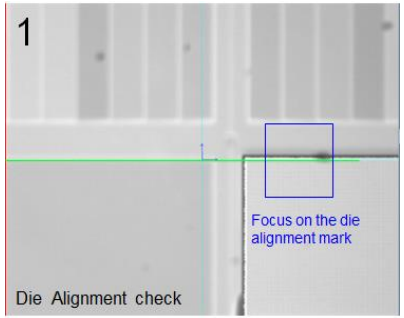


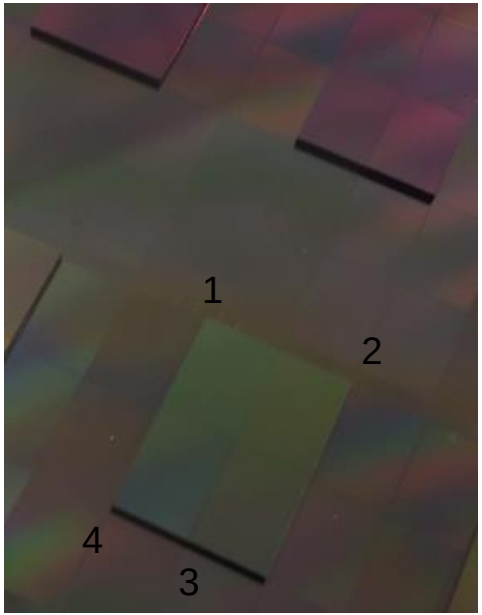


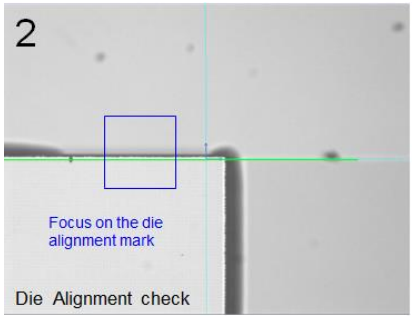
Pad Size 4 µm – 1µm

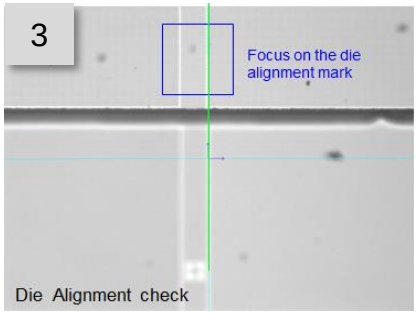
Pitch 8,8 µm – 2 µm

Co-D2W Bonding | Process Results – Hybrid Bonding





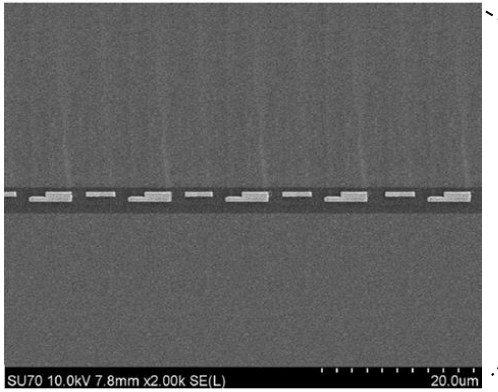


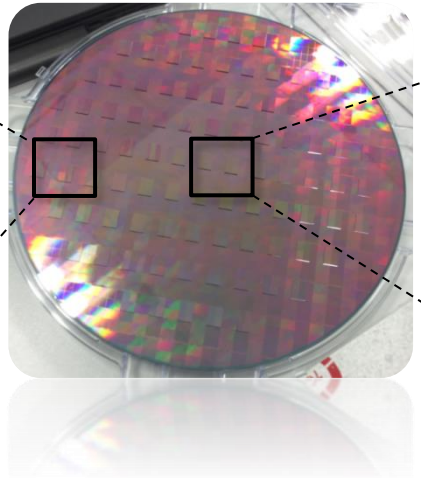


Demonstrator	Die Dimension	Placement accuracy x 3σ	Placement accuracy Y 3σ
A	5mm x 7mm	< 2 µm	< 2 µm
B	10mm x 14mm		

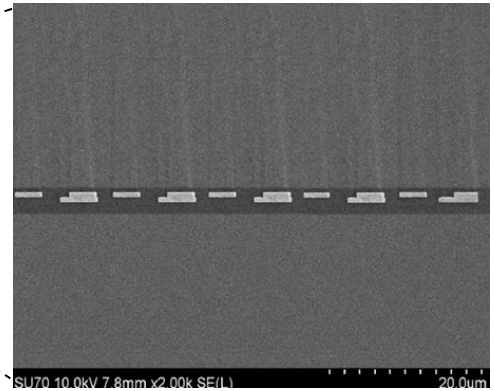
Co-D2W Bonding | Process Results – Hybrid Bonding

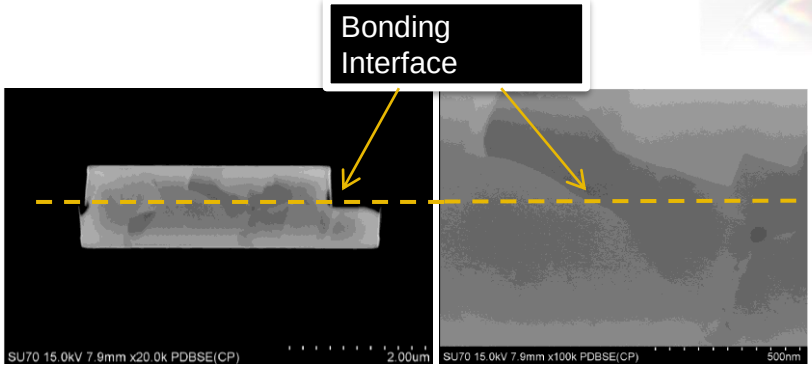
Edge Die





Center Die

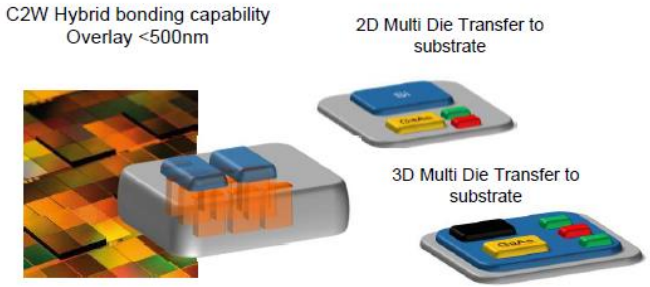




→ High Die transfer rate and alignment accuracy < 2µm could be demonstrated by collective die-to-wafer bonding process

→ Cross sectional analysis shows mechanical contact of the bonding pads and Cu grain growth across the bonding interface

2D and 3D Multi Die transfer



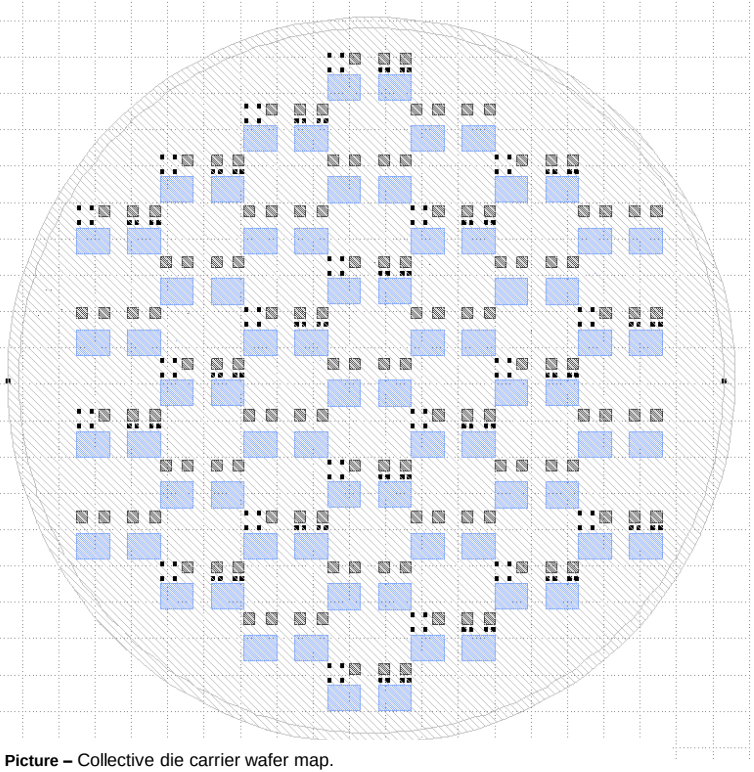
Demonstrator A

Target wafer: 200mm Thermal Oxide wafer

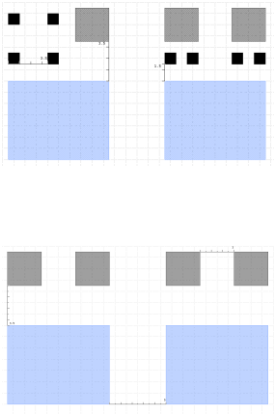
Collective carrier wafer: 200mm Bare Silicon wafer

Die sizes:

- 1x1mm x350µm dies
- 3x3mm x350µm dies
- 7x9mm x350µm dies



Picture – Collective die carrier wafer map.

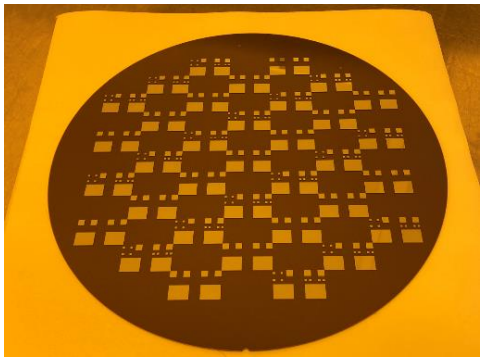


Picture – Collective die carrier wafer map – die detail.

Co-D2W Bonding | Process Results – Multi Die - Direct Bonding

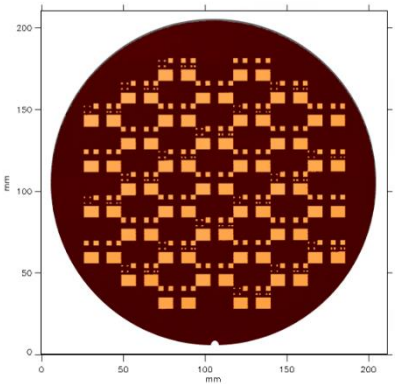
Post collective carrier preparation inspection

- A high-resolution die height variation (DHV) measurement was performed on the collective carrier with dies after placement using a chromatography sensor to evaluate the die uniformity / distribution.
- A die height variation < 3µm could be observed after collective die carrier preparation.

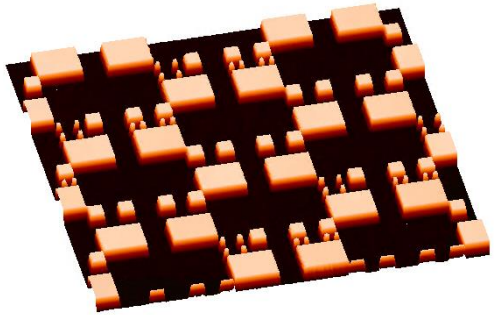


Picture – Collective die carrier wafers after die placement process.

a)

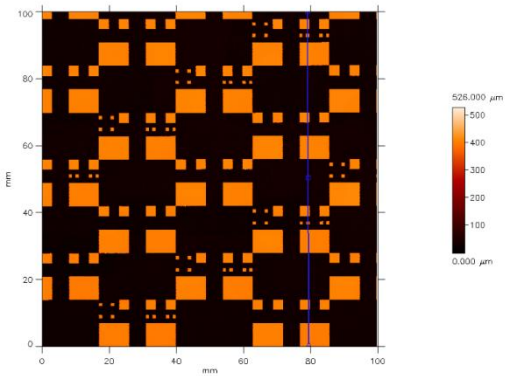


b)

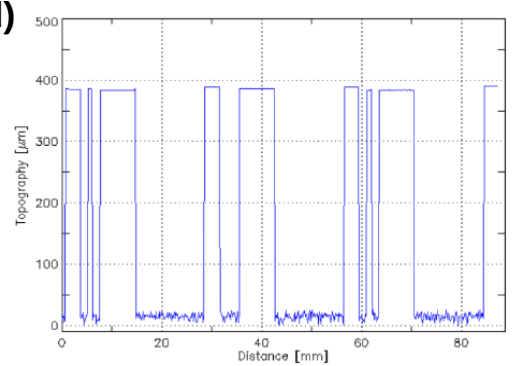


Die Height variation Measurement – a): Full scan – 2D collective carrier map**; b):** Detail scan – **3D collective carrier map.**

c)

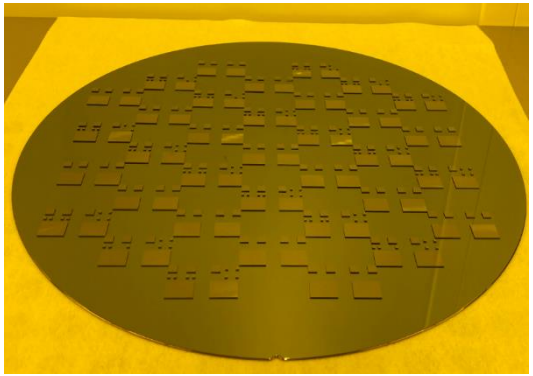


d)



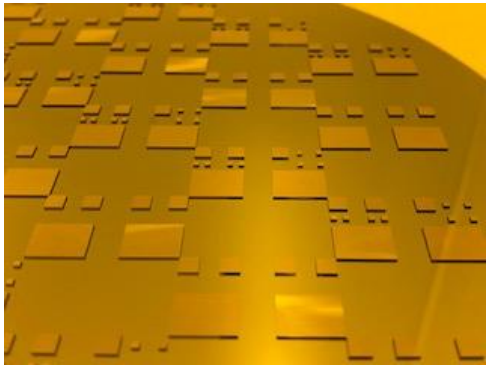
Die Height variation Measurement – a): Detail scan – 2D collective carrier map**; b):** Detail scan – DHV across the blue line.

Co-D2W Bonding | Process Results – Multi Die - Direct Bonding

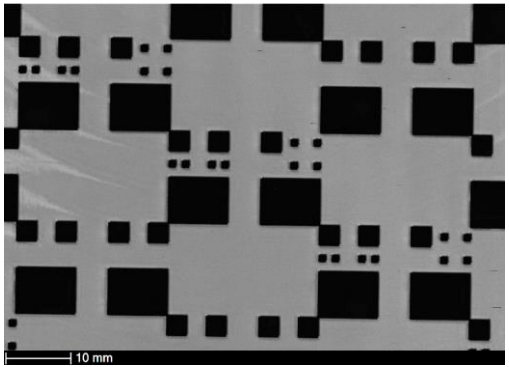


Picture – Target wafer with dies after die transfer process.

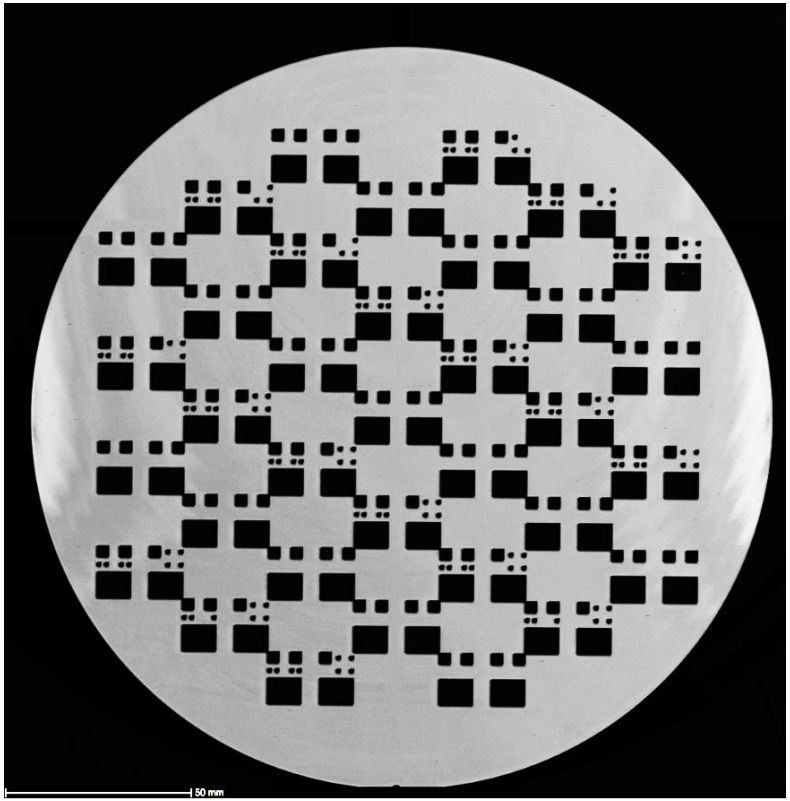
- High transfer yield including high bonding quality based on Scanning Acoustic microscope images (C-SAM) could be achieved.



Picture – Target wafer with dies after die-to-wafer bonding process – die detail..



C-SAM inspection – Post annealing inspection – detail scan.



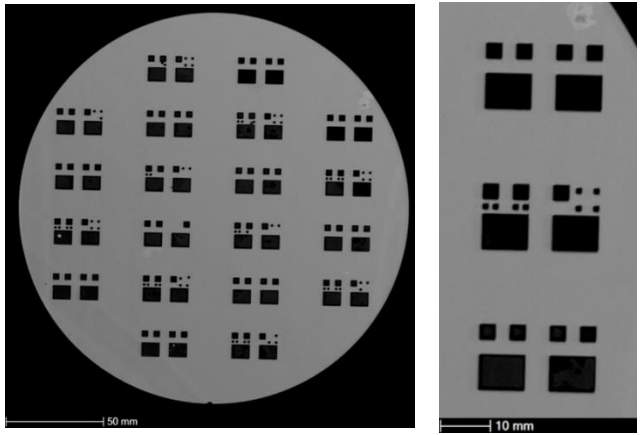
C-SAM inspection – Post annealing inspection – full scan.

Collective Die-to-Wafer (Co-D2W) Bonding | Metrology

Metrology // Co-D2W Bonding

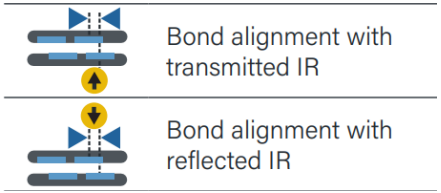
- **Post Co-D2W Bonding inspection:**
  - EVG50® - Die transfer rate
  - EVG40®NT (2) – D2W alignment verification
  - C-SAM – Bond quality

D2W Bonding interface:

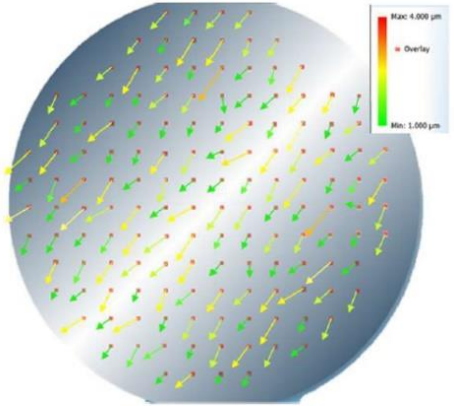


Picture – C-SAM inspection post D2W bonding.

D2W alignment verification

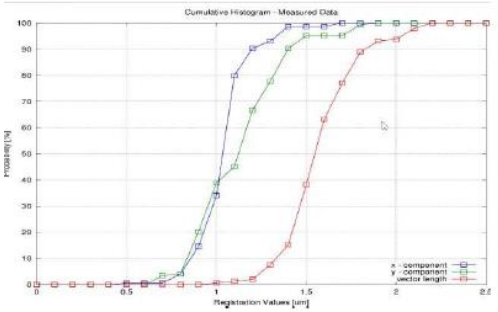


D2W + W2W alignment accuracy can be checked by TIR or RIR.



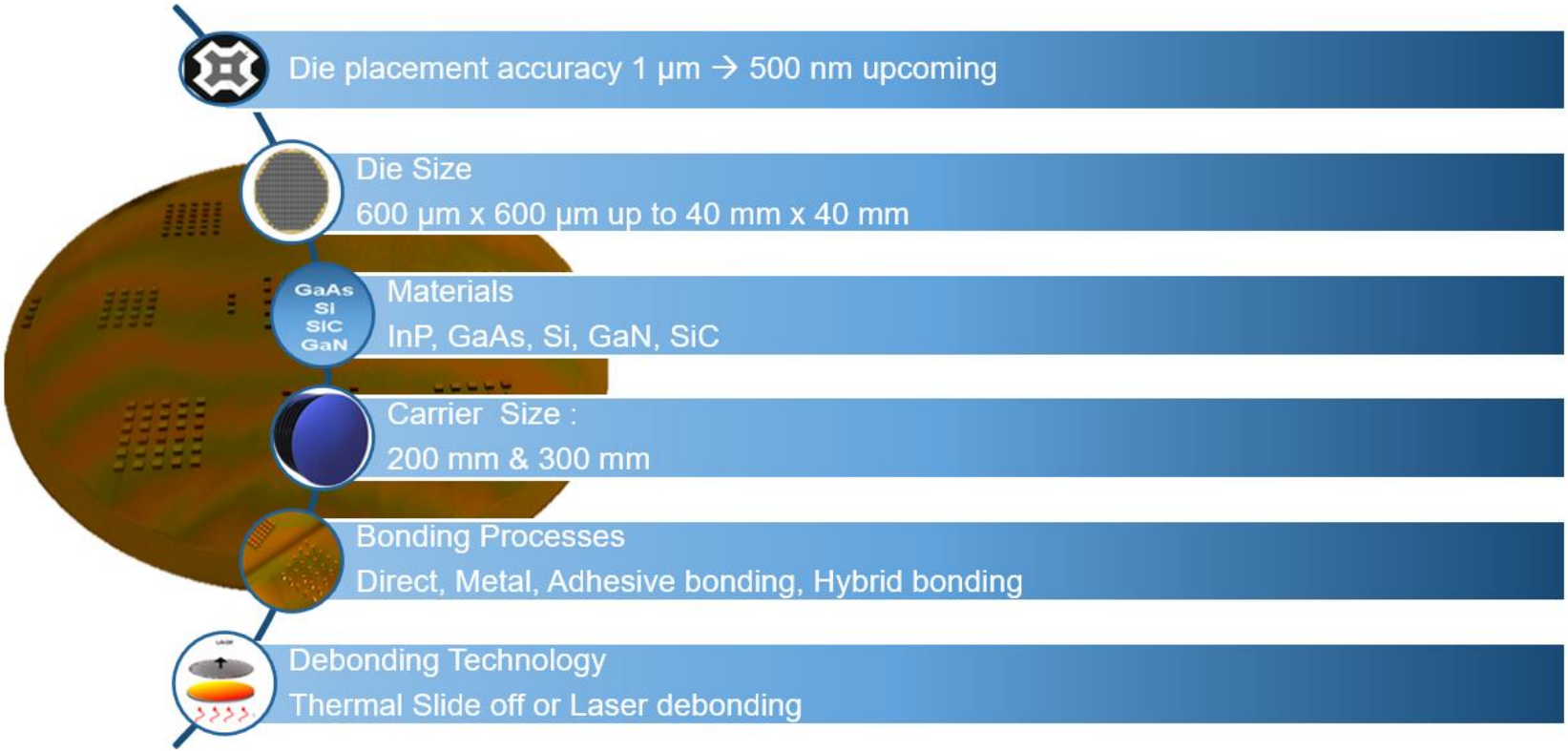
EVG40NT Die placement accuracy map post bonding

Post Bond Alignment accuracy Cumulative Plot



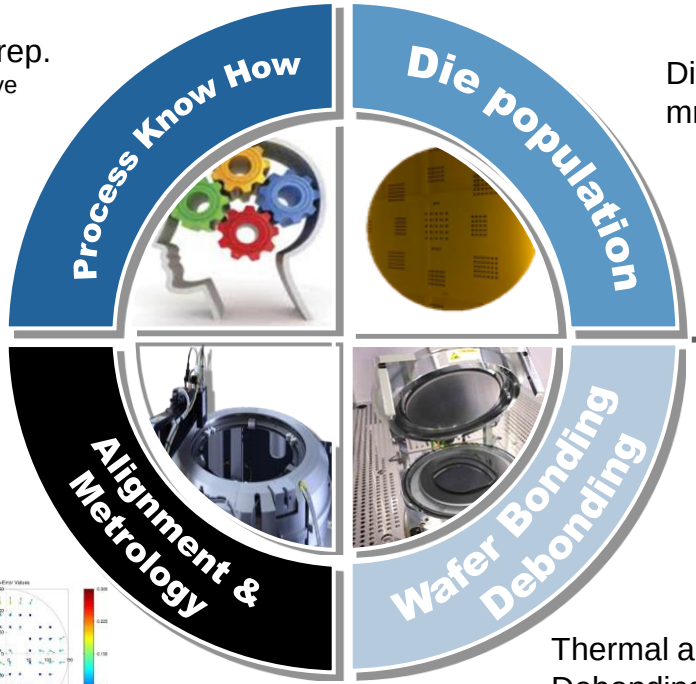
Summary & Outline

Die-to-Wafer Bonding I Die Transfer Capabilities @EVG

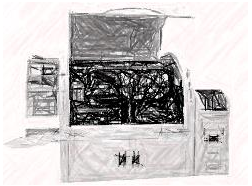


The efficient chiplet integration requires a combination of pick and place processes with wafer level proceesing and bonding to keep beeing succesful

Collective Die Carrier prep.
- Temporary Bonding Adhesive
- Protection layer selection

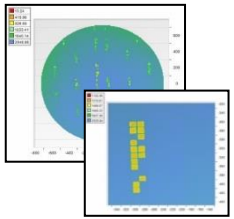


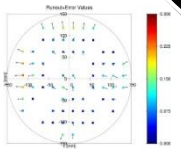
Die population on 200 mm & 300 mm Carrier



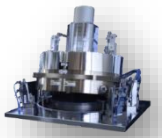
Incoming Die height &
Die thickness uniformity

Transfer rate





Hybrid Bonding
Direct Bonding
TC Bonding



Thermal and UV Laser Debonding capability

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